



Feature

- 100% EAS Guaranteed
- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

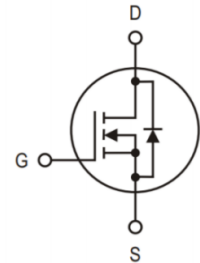
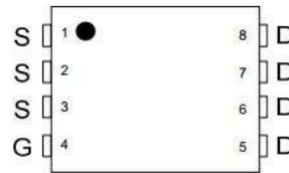
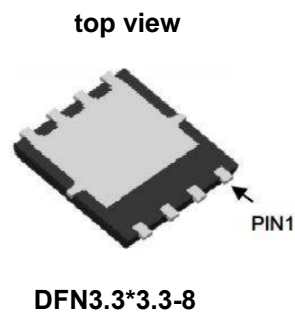
Product Summary



V_{DS}	30	V
$R_{DS(on),typ} V_{GS}=10V$	4.8	m Ω
I_D	55	A

Application

- Power Management in Inverter System



Maximum ratings, at $T_A=25\text{ }^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	30	V
I_S	Diode continuous forward current	$T_C=25^\circ\text{C}$ 55	A
I_D	Continuous drain current @ $V_{GS}=10V$	$T_C=25^\circ\text{C}$ 55	A
		$T_C=100^\circ\text{C}$ 35	A
I_{DM}	Pulse drain current tested ①	$T_A=25^\circ\text{C}$ 110	A
EAS	Avalanche energy, single pulsed ②	105	mJ
P_D	Maximum power dissipation	$T_C=25^\circ\text{C}$ 40	W
V_{GS}	Gate-Source voltage	± 20	V
MSL		Level 3	
T_{STG}, T_J	Storage and junction temperature range	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JL}$	Thermal Resistance, Junction-to-Lead	40	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	70	$^\circ\text{C/W}$



Typical Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	30	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current(T _J =25°C)	V _{DS} =30V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _J =125°C)	V _{DS} =30V, V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.0	1.5	2.5	V
R _{DS(ON)}	Drain-Source On-State Resistance ③	V _{GS} =10V, I _D =30A	--	4.8	6	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance ③	V _{GS} =4.5V, I _D =20A	--	7.5	12	mΩ
Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz		3105		pF
C _{oss}	Output Capacitance			410		pF
C _{rss}	Reverse Transfer Capacitance			305		pF
R _g	Gate Resistance	f=1MHz	--	1.6	--	Ω
Q _g	Total Gate Charge	V _{DS} =15V, I _D =15A, V _{GS} =10V	--	31.6	--	nC
Q _{gs}	Gate-Source Charge		--	6.07	--	nC
Q _{gd}	Gate-Drain Charge		--	13.8	--	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =15V, I _D =20A, R _G =1.5Ω, V _{GS} =10V	--	11.2	--	nS
t _r	Turn-on Rise Time		--	49	--	nS
t _{d(off)}	Turn-Off Delay Time		--	35	--	nS
t _f	Turn-Off Fall Time		--	7.8	--	nS
Source- Drain Diode Characteristics @ T_J = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =2A, V _{GS} =0V	--	0.8	1.0	V
t _{rr}	Reverse Recovery Time	T _J =25°C, I _{sd} =10A, V _{GS} =0V	--	20	--	nS
Q _{rr}	Reverse Recovery Charge	di/dt=500A/μs		11.5		nC

NOTE:

- ① Repetitive rating; pulse width limited by max. junction temperature.
 ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.1mH, R_G = 25Ω, I_{AS} = 42A, V_{GS} = 10V. Part not recommended for use above this value
 ③ Pulse width ≤ 300μs; duty cycle ≤ 2%.



Typical Characteristics

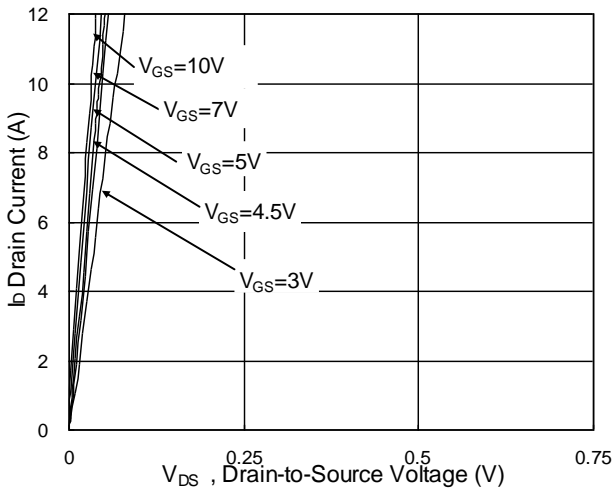


Fig.1 Typical Output Characteristics

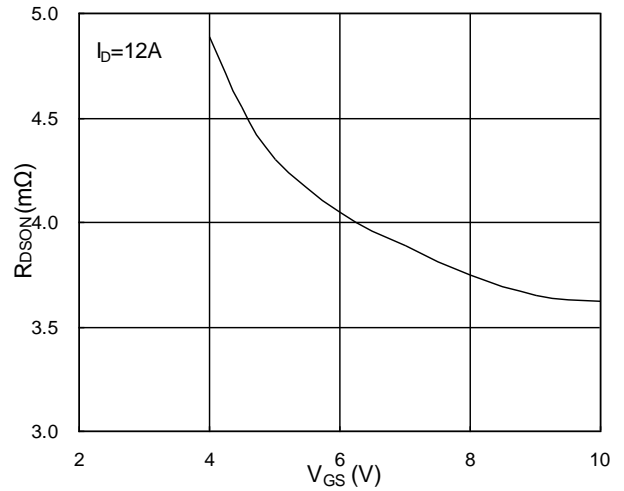


Fig.2 On-Resistance vs. G-S Voltage

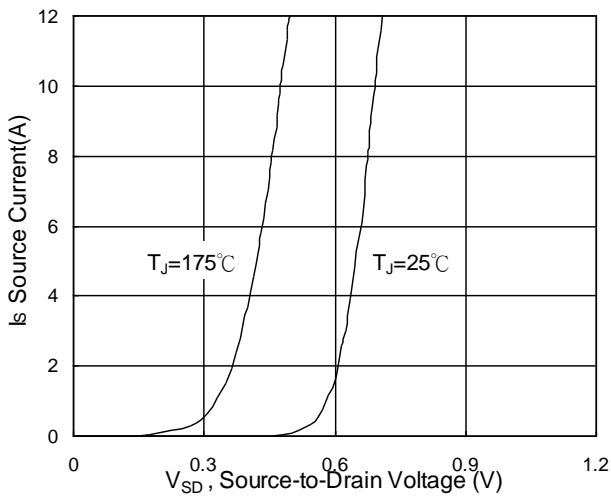


Fig.3 Forward Characteristics of Reverse

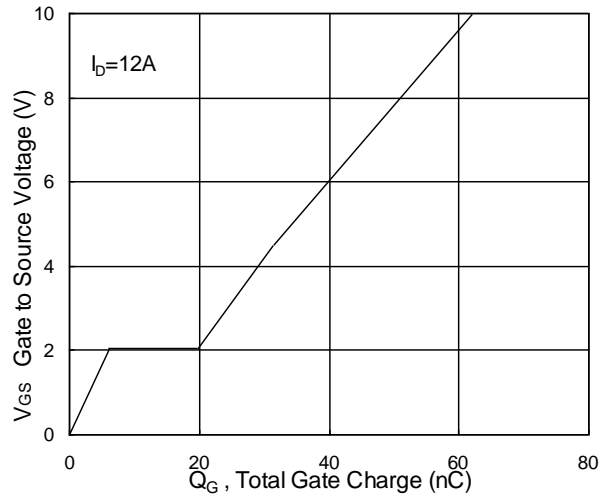


Fig.4 Gate-Charge Characteristics

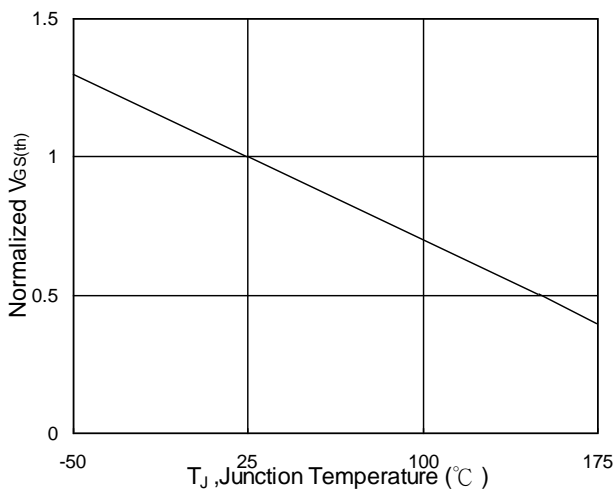


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

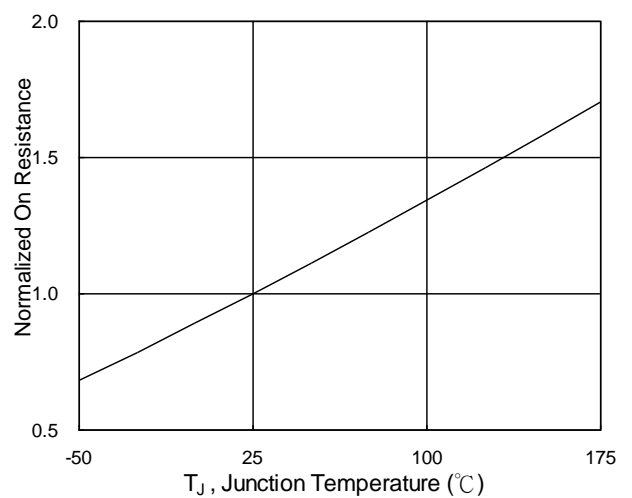


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

Typical Characteristics

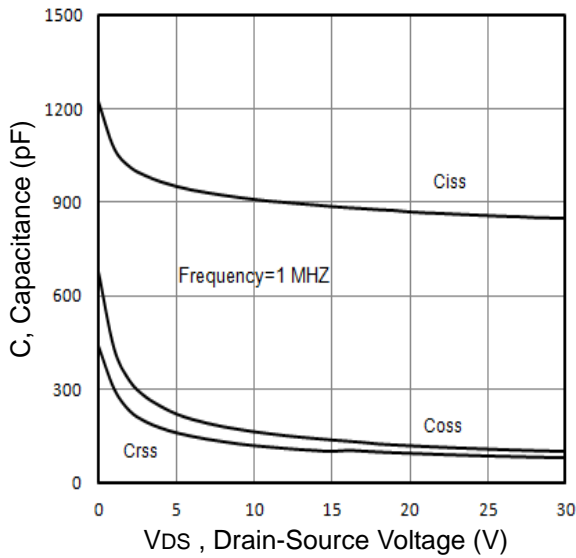


Fig7. Typical Capacitance Vs. Drain-Source Voltage

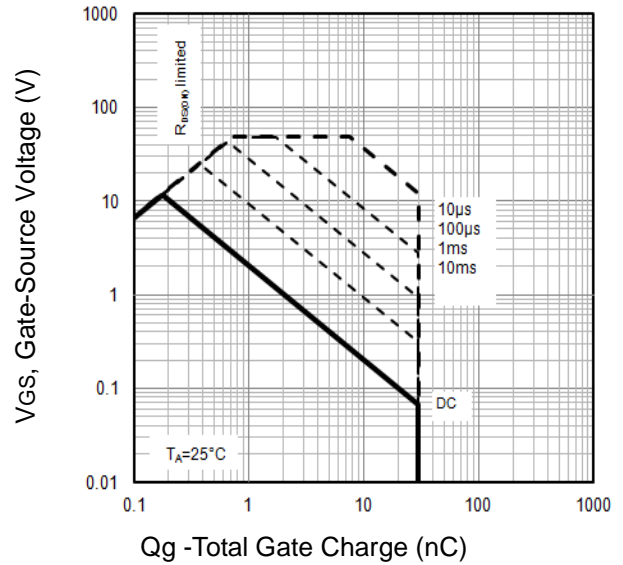
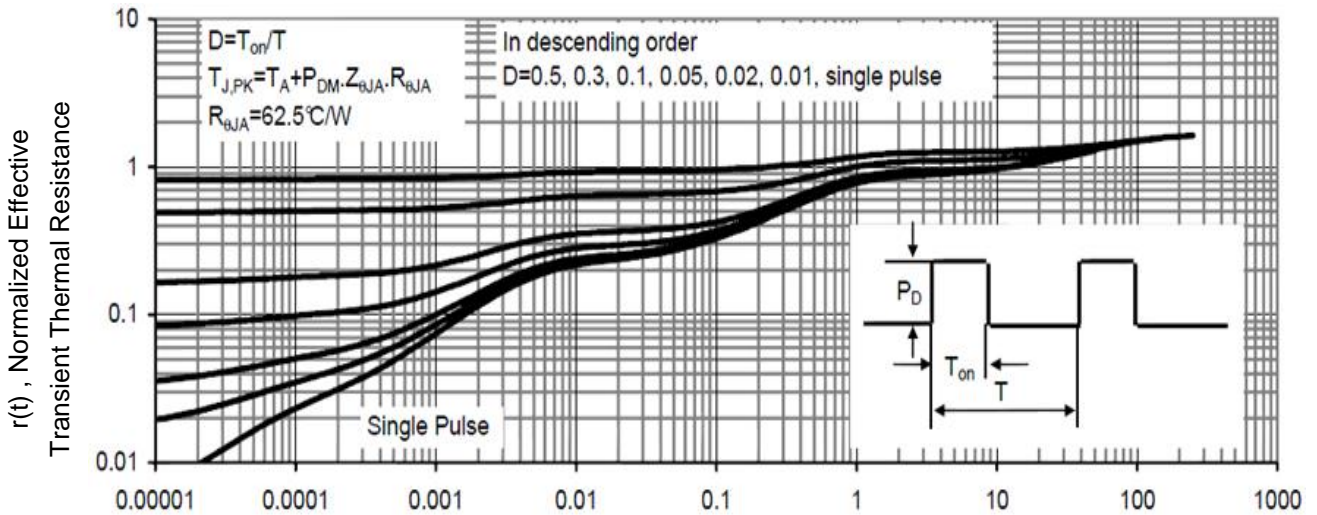


Fig8. Typical Gate Charge Vs. Gate-Source Voltage



T1, Square Wave Pulse Duration(sec)

Fig9. T1, Transient Thermal Response Curve

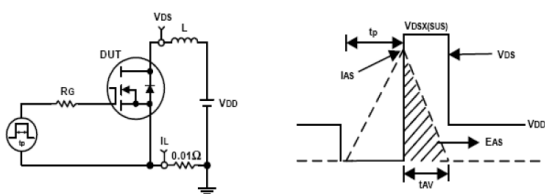


Fig10. Unclamped Inductive Test Circuit and waveforms

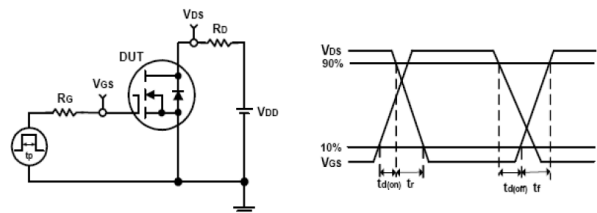
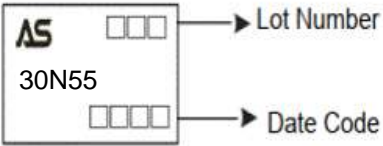


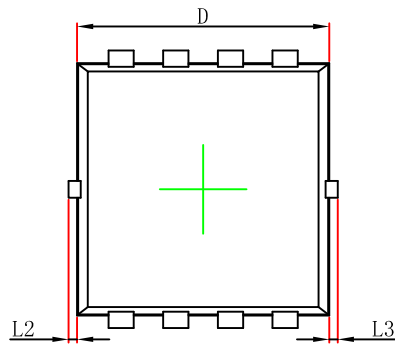
Fig11. Switching Time Test Circuit and waveforms

Ordering and Marking Information

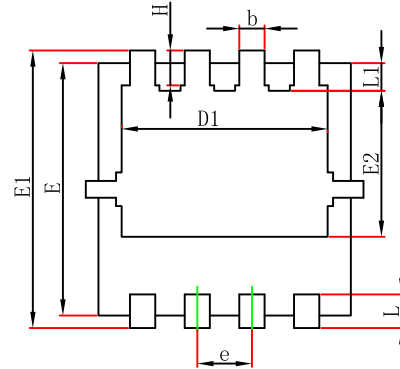
Device	Marking	Package	Packaging	Quantity
ASDM30N55E-R	30N55	DFN3.3*3.3-8	Tape&Reel	5000

PACKAGE	MARKING
DFN3.3*3.3-8	 <p>AS □□ → Lot Number 30N55 □□□□ → Date Code</p>

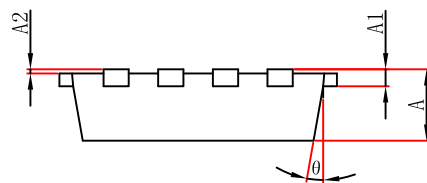
DFN 3.3×3.3 -8 (P0.65T0.80) PACKAGE OUTLINE DIMENSIONS



Top View
[顶视图]



Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°

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