Features

- Build-in 13mΩ/ 45V MOSFET
- Low current consumption
- Up to 70KHz operation frequency
- 1.2-Ω Sink,3.0-Ω Source Gate-Drive Impedances
- 50ns turn-off propagation delay
- VCC range from 3V to 6V
- VCC OVP Clamping
- Cycle by Cycle MOT Check Circuit prevents multiple false trigger Gate pulses
- DCM and CrCM operation
- SOP8 Package

Applications

- 5V AC-DC adaptors
- Battery Powered systems
- Digital Cameras Charger

General Description

SP6502FL is a smart secondary-side switch IC designed for isolated fly-back system. The IC emulate the behavior of Schottky diode rectifier for reduces power dissipation. SP6502FL works in DCM and CrCM operation modes. Ruggedness and noise immunity are accomplished using an advanced blanking scheme and double-pulse suppression which allow reliable operation in all operating modes.

SP6502FL senses the build-in MOSFET drain-source voltage, and output ideal drive signal with less external components. It only provides high performance solution for 5V output voltage application.

Simplified Application

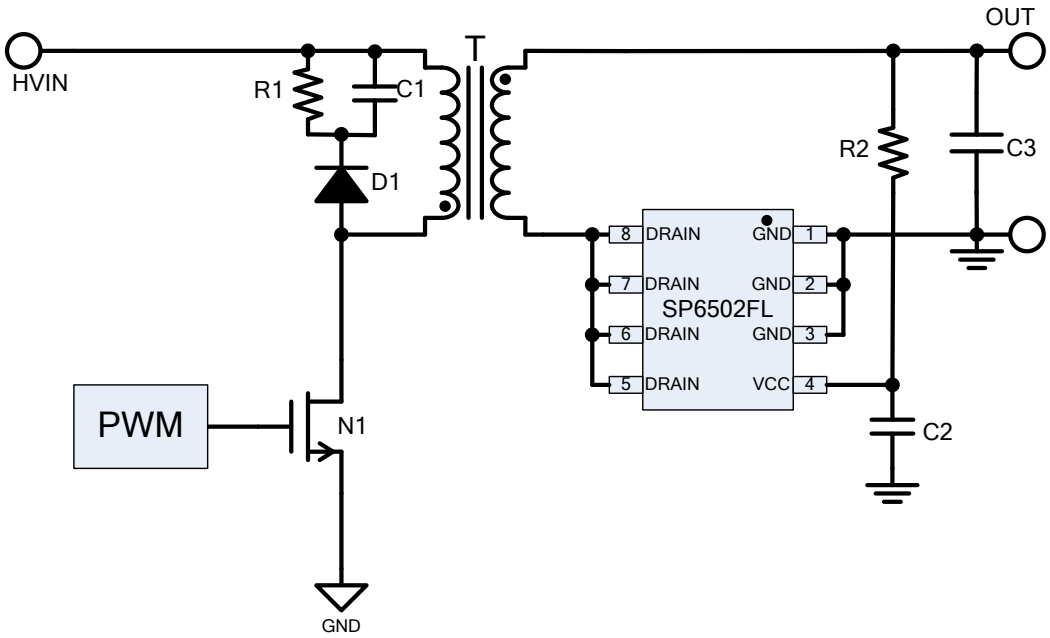
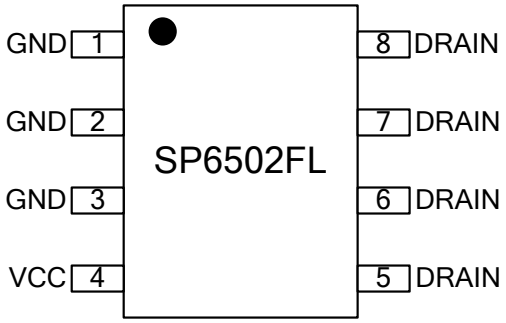


Figure 1. Simplified Application of SP6502FL

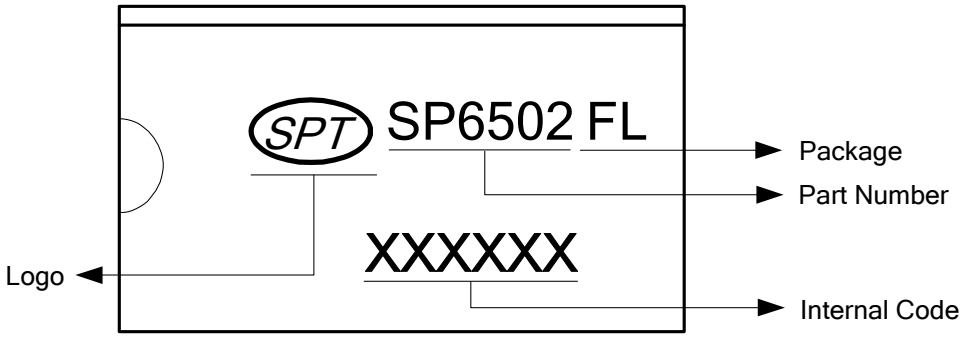
Pin Configuration and Functions



Pin No.	Pin Name	Function Description
1、2、3	GND	Power Ground, Return for MOSFET Source
4	VCC	Inner Power Supply, Connect Capacitor to Ground
5、6、7、8	DRAIN	MOSFET Drain side

Ordering and Marking Information

Part Number	Package Description	Top Marking	Package Form
SP6502FL	SOP8, Pb-free	SP6502FL	SOP8



Package Dissipation Rating

Package	θ_{JC} （℃/W）	θ_{JA}（℃/W）
SOP8	50	130

Absolute Maximum Ratings

Symbol	Description	Value	Units
DRAIN	MOSFET Drain	-1 to 45	V
VCC	VCC Input Voltage	-0.3 to 7	V
T_J	Operating Junction Temperature	-40 to 125	℃
T_{stg}	Min/Max Storage Temperature	-55 to 150	℃
T_L	Lead Temperature (Soldering. 10secs)	260	℃

Note: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Description	Value	Units
VCC	VCC Supply Voltage	5	V
	VCC bypass Capacitor	>1	uF
Fsw	Switch Frequency	<70	KHz
DRAIN	MOSFET Drain Voltage	-0.6~45	V

Block Diagram

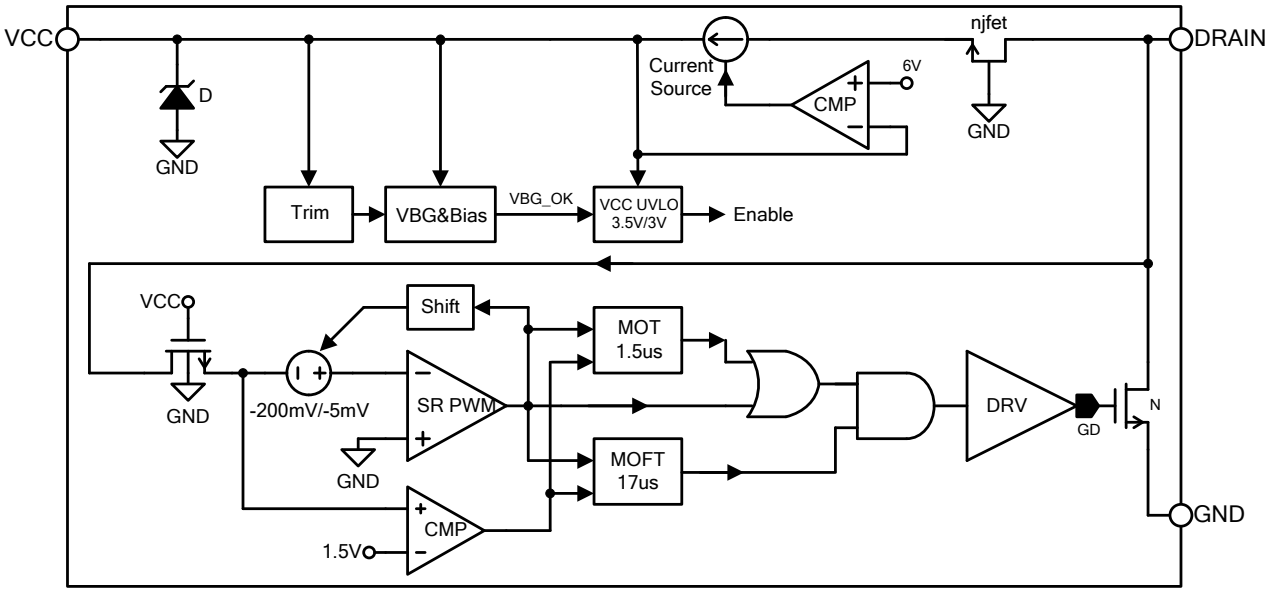


Figure 2. Block diagram of SP6502FL

Electrical Characteristics

VCC=5V, TA=25℃, unless otherwise noted.

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
VCC Section						
ICC	Quiescent Current			110	150	uA
V_{CC_ON}	VCC ON Voltage	VCC Going Up	3.4	3.5	3.6	V
V_{CC_OFF}	VCC OFF Voltgae	VCC Going Down	2.9	3	3.1	V
V_{CC_OVP}	VDD over voltage protection		6	6.3	6.6	V
SR Section						
MOT	Minimum ON Time			1.5	2	us
MOFT	Minimum OFF Time			17		us
V_{THON}	SR ON threshold	SR Voltage down		-200		mV
V_{THOFF}	SR OFF threshold	SR Voltage up		-5		mV
V_{THRST}	SR Reset threshold	SR Voltage up		1.5		V
VD Section						
ID	VD Current Source	VD=30V，VCC=0V		15		mA
Inner GD Section						
Rgd_up	Gate Pull up Resistance			3		Ω
Rgd_down	Gate Pull down Resistance			1.2		Ω
$F_{\_MAX}$	Maximum frequency		70			KHz
T_{DON}	Turn On Delay Time	SR down to GD=4V		85		ns
T_{DOFF}	Turn OFF Delay Time	SR up to GD=1V		45		ns
T_{GDR}	Turn On Rising Time	From 1V to 4V, CL=6.3nF		70		ns
T_{GDF}	Turn Off Falling Time	From 4V to 1V, CL=6.3nF		40		ns
MOS Section						
RDSON	Static drain to source on resistance	VCC=5V		13		mΩ

Application Example

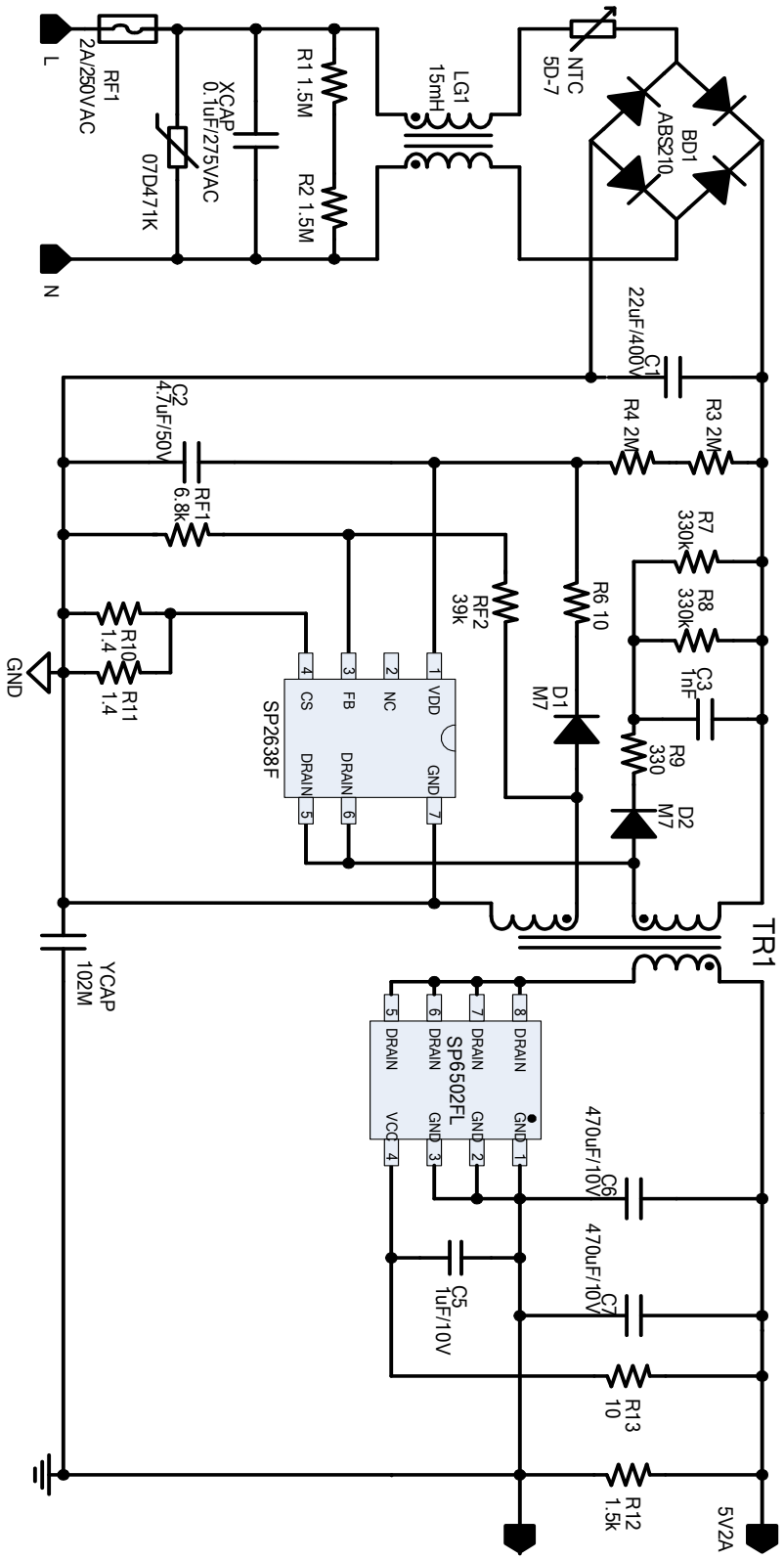


Figure 3. Schematic of Typical Application Circuit

Functional Description

SP6502FL detects the internal MOSFET drain-source voltage (VDS). When the drain voltage is lower than the turn-on threshold voltage (V_{THON}), it outputs a positive drive voltage after a turn-on delay time (T_{DON}). The internal MOSFET will turn on and the current will transfer from the body diode into the internal MOSFET's channel, then lower conduction loss can be achieved. In the process of internal MOSFET channel current decreasing linearly toward zero, the drain-source voltage rises synchronically. When it rises over the turn off threshold voltage (V_{THOFF}), SP6502FL pulls down the internal MOSFET gate voltage to zero after a turn off delay time (T_{DOFF}). See Figure.4

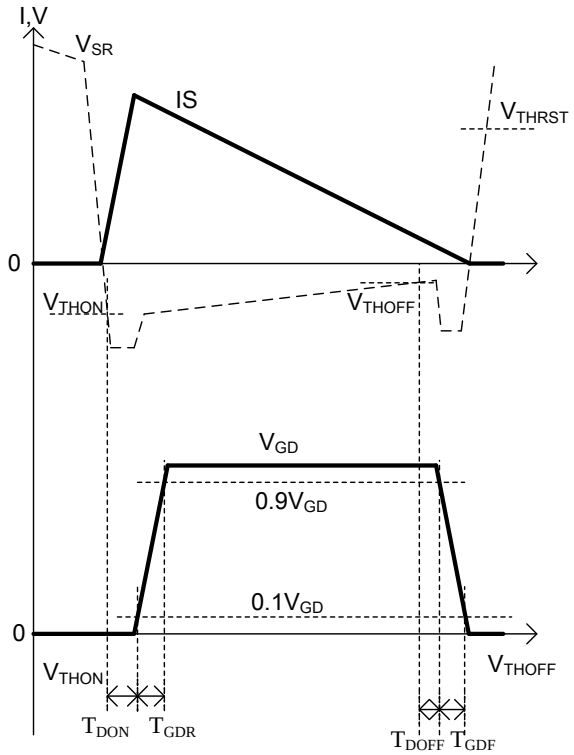


Figure 4. Typical Waveforms of SP6502FL

Power Supply

The IC supply voltage is monitored by the under lockout circuit. It is possible to turn off the IC by pulling VCC pin below the minimum turn off threshold voltage, without damaging the IC. To prevent noise problems, a bypass ceramic capacitor connected to VCC and GND should be placed as close as possible to IC. This pin is internally clamped at 6.3V.

UVLO Mode

The IC remains in the UVLO condition until the voltage on the VCC pin exceeds the VCC turn on threshold voltage V_{CC_ON}. During the time the IC remains in the UVLO state, the gate drive circuit is inactive and the IC draws a quiescent current of ICC START. The UVLO mode is accessible from any other state of operation whenever the IC supply voltage condition of VCC < V_{CC_OFF} occurs.

Minimum On Time

When the controlled internal MOSFET gate is turned on, some ringing noise is generated. The minimum on time blanks the V_{THOFF} comparator, keeping the controlled internal MOSFET on for at least the minimum on time. If V_{THOFF} falls below the threshold before minimum on time expires, the internal MOSFET will keep on until the end of the minimum on time.

Drain Voltage Inner Sense

DRAIN pin is used to sense the internal MOSFET Drain voltage. This is a high voltage pin and particular care must be taken in properly routing the connection to the internal MOSFET drain side.

Normal Mode

The IC enters in normal operating mode once the UVLO voltage has been exceeded. When the IC enters Normal Mode from UVLO Mode, the GATE output is disabled (stays low) until V_{SR} exceeds V_{THRST} to activate the gate. This ensures that the GATE output is not enabled in the middle of a switching cycle. This logic prevents any reverse currents across the device due to minimum on time function in the IC. The gate will continuously drive the SR internal MOSFET after this one-time activation. The Cycle by Cycle MOT protection circuit is enabled in Normal Mode.

MOT Protection Mode

If the secondary current conduction time is shorter than the MOT (Minimum On Time) setting, the next driver output is disabled. This function can avoid reverse current that occurs when the system works at very low duty-cycles or at very light/no load conditions and reduce system standby power consumption by disabling GATE outputs. The Cycle by Cycle MOT Check circuit is always activated under Normal Mode and MOT Protection Mode, so that the IC can automatically resume normal operation once the load increases to a level and the secondary current conduction time is longer than MOT.

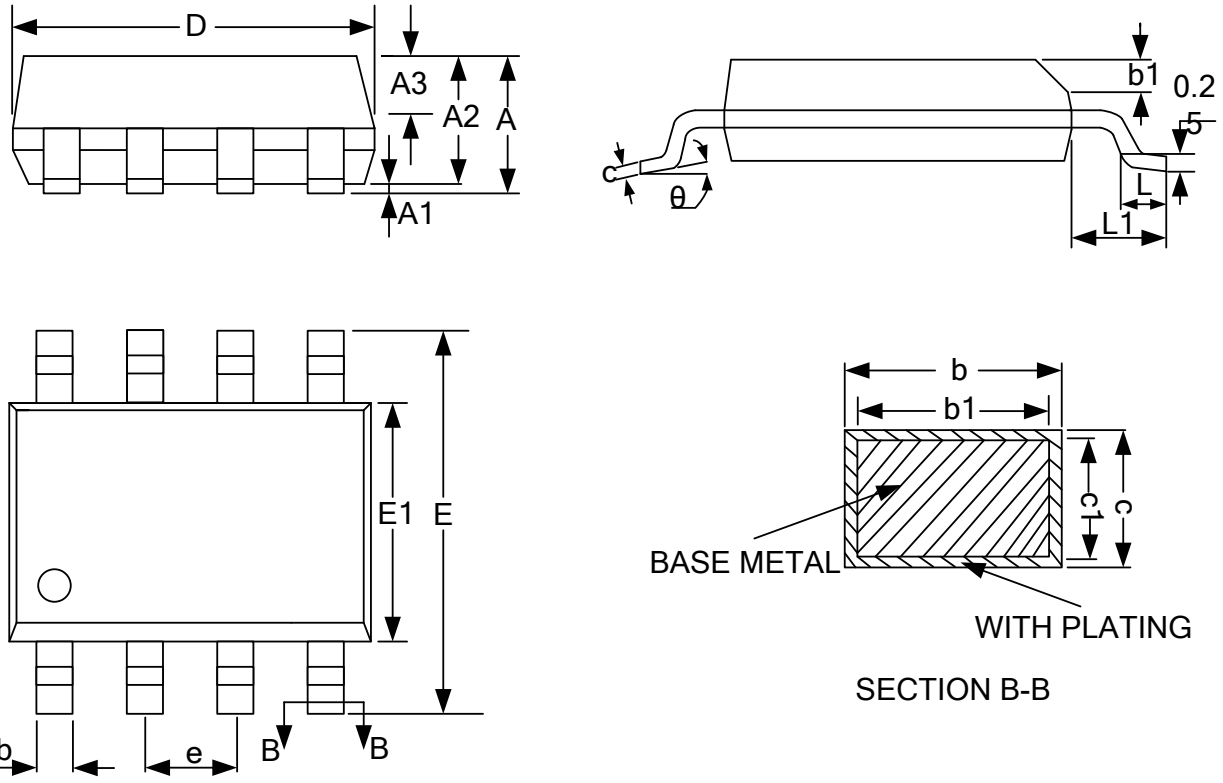
Turn-on phase

When the conduction phase of the SR internal MOSFET is initiated, current will start flowing through its body diode, generating a negative VDS voltage across it. The body diode has generally a much higher voltage drop than the one caused by the internal MOSFET on resistance and therefore will trigger the turn-on threshold V_{THON}. At that point, SP6502FL will drive the gate of internal MOSFET on, which will in turn cause the conduction voltage VDS to drop down. This drop is usually accompanied by some amount of ringing, that can trigger the input comparator to turn off, hence, a Minimum On Time (MOT) blanking period is used that will maintain the power internal MOSFET on for a minimum amount of time.

DCM/CrCM Turn-off phase

Once the SR internal MOSFET has been turned on, it will remain on until the rectified current will decay to the level where internal MOSFET VDS will cross the turn-off threshold V_{THOFF}. This will happen differently depending on the mode of operation. In DCM the current will cross the threshold with a relatively low dI/dt. Once the threshold is crossed, SP6502FL will turn off gate and the current will start flowing again through the body diode, causing the VDS voltage to jump negative. Depending on the amount of residual current, internal MOSFET VDS may trigger once again the turn on threshold. For this reason V_{THON} is blanked for a certain amount of time (T_{BLANK}) after V_{THOFF} has been triggered. The blanking time is internally set. As soon as internal MOSFET VDS crosses the positive threshold V_{THRST}, the blanking time is terminated and the IC is ready for next conduction cycle.

Package Information（Unit:mm）



SYMBOL	MILLIMETER			SYMBOL	MILLIMETER		
	MIN	NOM	MAX		MIN	NOM	MAX
A	—	—	1.75	D	4.70	4.90	5.10
A1	0.05	—	0.15	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e	1.27BSC		
b	0.39	—	0.48	h	0.25	—	0.50
b1	0.38	0.41	0.43	L	0.50	—	0.80
c	0.21	—	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0	—	8°

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- In developing your designs, please ensure that Si-Power products are used within specified operating ranges as set forth in the most recent Si-Power products specifications.
- The information contained herein is subject to change without notice.

Revision History

Change Date	Rev.	Description of Change
2017/2/14	1.0	Datasheet Release